IN THE CLAIMS:

Please cancel Claims 25-30 without prejudice and without disclaimer of subject matter.

Please amend Claim 24 as shown.

Please add Claims 30-31 as shown.

1-23. (Canceled)

24. (Currently Amended) A method of forming a trench DMOS transistor device comprising:

providing a substrate of a first conductivity type, said substrate acting as a common drain region for said device;

depositing an epitaxial layer of said first conductivity type over said substrate, said epitaxial layer having a lower majority carrier concentration than said substrate;

forming a body region of a second conductivity type within an upper portion of said epitaxial layer;

etching a trench extending into said epitaxial layer from an upper surface of said epitaxial layer;

forming an insulating layer lining at least a portion of said trench;

forming a conductive region within said trench adjacent said insulating layer;

forming a source region of said first conductivity type within an upper portion of said body region and adjacent said trench; and

forming a ~~low resistivity deep region extending into said device from an upper surface of said epitaxial layer, said deep region~~ metal drain contact that extends from an upper surface of the epitaxial layer through the epitaxial layer, and into contact with the substrate, said metal drain contact acting to provide electrical contact with said substrate; and

forming a metallic source contact adjacent an upper surface of the source region, and a metallic gate contact adjacent an upper surface of the conductive region in a termination region remote from the source region.

25-30. (Canceled)

31. (New) A method of forming a trench DMOS transistor device comprising:

providing a substrate of a first conductivity type, said substrate acting as a common drain region for said device;

depositing an epitaxial layer of said first conductivity type over said substrate, said epitaxial layer having a lower majority carrier concentration than said substrate;

forming a body region of a second conductivity type within an upper portion of said epitaxial layer;

etching a trench extending into said epitaxial layer from an upper surface of said epitaxial layer;

forming an insulating layer lining at least a portion of said trench;

forming a conductive region within said trench adjacent said insulating layer;

forming a low resistivity deep region extending into said device from an upper surface of said epitaxial layer, said deep region acting to provide electrical contact with said substrate; and

forming a source region of said first conductivity type within an upper portion of said body region and adjacent said trench, wherein said step of forming a source region also forms a region of first conductivity within the low resistivity deep region.

32. (New) The method of claim 31, wherein the region of first conductivity formed within the low resistivity deep region is formed by implantation and diffusion.